NO. 13

PATENT ABSTRACTS OF JAPAN

(11)Publication number : 07-046202
(43)Date of publication of application : 14.02.1995

(51)Int.Cl. H04B 17/00
H04B 7/02
H04L 27/18

(21)Application number : 05-191235
(22)Date of filing : 02.08.1993

(71)Applicant : JAPAN RADIO CO LTD
(72)Inventor : TANIGUCHI TORU

(54) METHOD AND CIRCUIT FOR DETECTING FADING

(57)Abstract:
PURPOSE: To improve the fading detection sensitivity in a 4 PSK receiver.
CONSTITUTION: The circuit is provided with a phase identification circuit 24 identifying a phase of a base fond output of a 4PSK demodulator 10. A timing resulting from delaying an eye aperture timing obtained from a clock extract circuit 18 at a delay circuit 42 is used for a sampling timing for the phase identification circuit 24 by a sample-and-hold circuit 40. When the sampling timing (observed timing) by the sample-and-hold circuit 40 is shifted by the delay circuit 42, fading appears at an output of the phase identification circuit 24 as a rotation or torsion of a constellation. The phase identification circuit 24 receives no effect of level fluctuation of an input to the 4PSK demodulator 10 or deterioration in the modulation characteristic or the like.